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Comparison of two PWM schemes for SiC device based split output converters in high-switching-frequency applications

Qingzeng Yan^{*†}, Xibo Yuan^{*}, Xiaojie Wu[†]

^{*}Department of Electrical and Electronic Engineering, University of Bristol, Bristol BS8 1UB, UK.

[†]School of Information and Electrical Engineering, China University of Mining and Technology, Xuzhou 221116, China.
Email: yqz2009@163.com

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Abstract

The adoption of the fast-switching silicon carbide (SiC) devices in the conventional two-level voltage source converters can bring issues such as the crosstalk effect, the high turn-on losses, the electromagnetic interference (EMI), etc. The split output converter can decouple the upper SiC MOSFET from the lower SiC MOSFET in the same phase leg with suppressed crosstalk effect, lower turn-on losses, and reduced EMI. These advantages enable the split output converter to operate at high switching frequencies (e.g. 100kHz). However, as a limiting factor at high switching frequencies, the dead time in the conventional pulse width modulation with synchronous rectification (SRPWM) can cause low-frequency voltage/current harmonics and reduce the linear modulation region with lower dc-link voltage utilization. While the current direction related pulse width modulation (CDPWM) has no such problems due to the abandon of the dead time. A detailed comparison between the SRPWM and the CDPWM is carried out in this paper regarding harmonics, control, and efficiency. Both the analysis and the experimental results verify that, the CDPWM is superior to the SRPWM for the SiC device based split output converters in high-switching-frequency applications.

1 Introduction

With the fast-switching silicon carbide (SiC) devices, the power converter can operate at higher switching frequencies with improved converter efficiency and power density [1]-[3]. However, regarding the standard two-level voltage source converter, the ultra-fast switching speed can intensify the interaction between the upper SiC MOSFET and the lower SiC MOSFET of the same phase leg ('crosstalk' effect [1]), and make the converter more susceptible with the parasitic elements in the power circuit [2]. The high dv/dt and di/dt can cause serious electromagnetic interference (EMI) problem. In addition, the turn-on losses of the SiC MOSFET can be increased by the charging current of the output capacitance and the reverse recovery current of the body diode in its complementary SiC MOSFET.

The split output converters [2], [3], which are also known as the dual-buck converters [4], can transcend the above limitations of the standard two-level converters in high-

switching-frequency applications, as seen in Fig. 1. $Q_1 \sim Q_6$ are SiC MOSFETs and $D_1 \sim D_6$ are SiC Schottky diodes; L_{load} is the load/filtering inductors. For the sake of clear descriptions, the auxiliary inductors connecting the two legs in one phase, e.g. L_{s1} and L_{s4} , are called 'split inductors'.

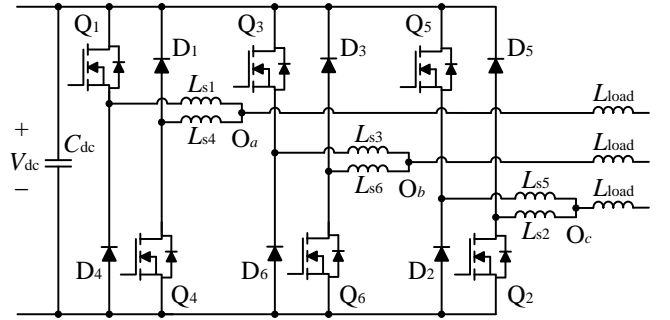


Fig. 1: Three-phase split output converter.

As seen in Fig. 1, the split inductors separate the upper SiC MOSFET from the lower SiC MOSFET. Consequently, the crosstalk effect can be attenuated with lower induced spurious gate voltage avoiding the potential shoot-through failure. The charging current of the output capacitance and the reverse recovery current of the body diode will be both buffered by the split inductors, resulting in lower turn-on losses of the SiC MOSFET. In addition, if regarding the nodes O_a , O_b , and O_c in Fig. 1 as the outputs of the converter, the dv/dt of the output voltage will be reduced with lower EMI.

The above advantages enable the split output converter to operate at high switching frequencies (e.g. 100kHz). The pulse width modulation (PWM) schemes for the split output converter in high-switching-frequency applications should be carefully selected. Regarding the converters based on SiC MOSFETs with bidirectional-conduction capability, using certain PWM schemes, there can be synchronous rectification mode where the freewheeling current is shared between the SiC MOSFET and the diode with improved efficiency [5]. Based on the features with or without synchronous rectification, the PWM schemes can be grouped into two basic categories: the PWM with synchronous rectification (SRPWM) [6] and the current direction related PWM without synchronous rectification (CDPWM) [4], [7]. The SRPWM and the CDPWM can further contain several kinds of modulations according to the modulation waves adopted, e.g. the sinusoidal PWM (SPWM), the space vector PWM (SVPWM), the discontinuous space vector PWM (DSVPWM) [4], etc.

With the fast switching SiC devices, the dead time in the SRPWM can be very short, making the dead time effect acceptable at low-switching frequencies. However, the output voltage errors caused by the dead time will be intensified as the switching frequency goes higher. The CDPWM without dead time can avoid the dead time effect existing in the SRPWM. Nevertheless, the implementation of the CDPWM requires the output current direction, which is challenging when the current is extremely small with noise and ripple at the zero crossing. This paper therefore aims to carry out a comparative study of the two PWM schemes regarding harmonics, control, and efficiency, and give a conclusion which PWM scheme is superior for the SiC device based split output converters at high switching frequencies.

2 Modulation mechanism analysis of the SRPWM and the CDPWM

The modulation mechanisms of the SRPWM and the CDPWM with sinusoidal modulation wave are illustrated in Fig. 2, where the frequency of the carrier is ten times that of the modulation wave to make the figure clear.

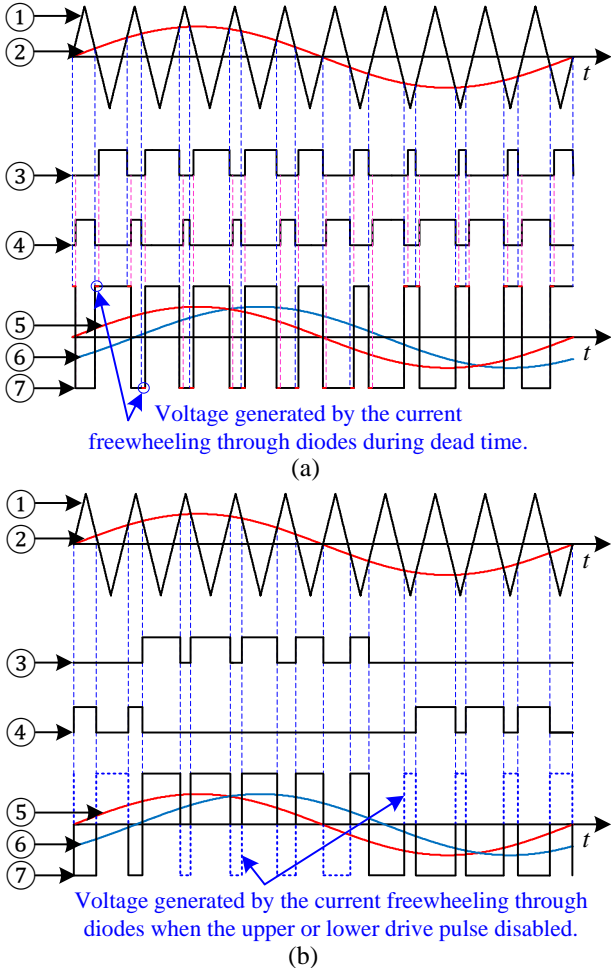


Fig. 2: Modulation mechanisms with sinusoidal modulation wave: (a) SRPWM and (b) CDPWM [①Carrier, ②Sinusoidal modulation wave, ③Upper drive pulse, ④Lower drive pulse, ⑤Fundamental voltage, ⑥Output current, ⑦Output voltage].

The SRPWM shown in Fig. 2(a) is the commonly used PWM scheme in two-level converters. If the sinusoidal modulation wave is larger than the carrier, the upper SiC MOSFET will turn on, otherwise the lower SiC MOSFET will turn on. The drive pulse in the current freewheeling stage will turn on the SiC MOSFET, making the circuit in the synchronous rectification mode where the freewheeling current is shared between the SiC MOSFET and the diode with improved efficiency [5]. A drawback of this modulation is the indispensable dead time for avoiding the shoot-through failure. During the dead time, the output voltage is generated by the current freewheeling through diodes, thus causing the voltage errors related to the output current direction [8], [9]. Although the dead time can be quite short with the fast-switching SiC MOSFETs, the dead time effect can still be serious at high switching frequencies (e.g. 100kHz).

As seen in Fig. 2(b), with the CDPWM, the drive pulse in half the fundamental period is disabled according to the current direction. For example, when the output current is positive, the lower drive pulse is disabled. During this time, the negative output voltage is generated by the current freewheeling through diodes, to guarantee the principle of equivalent accumulated impulse. Only one dead time is necessary to avoid the shoot through failure when alternating the enabled pulse at the current zero crossing. For the rest part of modulation, no dead time is required. Consequently, the output voltage/current will not be distorted by the voltage errors caused by dead time even at high-switching frequencies. In addition, the abandon of the dead time also reduces the possibility of the shoot-through failure [4].

3 Influence of the dead time and switching frequency on the linear modulation region

Apart from the nonlinear modulation caused by the overmodulation where the amplitude of the modulation wave is larger than that of the carrier [6], the dead time existing in the SRPWM can also lead to the nonlinear modulation. How the dead time and switching frequency affect the linear modulation region of the SRPWM will be analyzed in this section.

In the SRPWM, the modulation at the top of the modulation wave in one switching cycle is shown in Fig. 3, where T_s is the switching period; T_d is the dead time; u_{rm} and u_{cm} are the amplitudes of the modulation wave and the carrier, respectively. The modulation index M with the sinusoidal modulation wave can be defined as [6]

$$M = \frac{u_{rm}}{u_{cm}} \quad (1)$$

Based on the properties of similar triangles, (2) can be obtained as

$$\frac{T_i}{T_s} = \frac{u_{cm} - u_{rm}}{2u_{cm}} \quad (2)$$

As seen in Fig. 3, when T_i is smaller than T_d , the lower drive pulse will always be in low-state, making the converter in the nonlinear modulation region. Assuming $T_i = T_d$, the maximum

linear modulation index M_m can be derived from (1) and (2) as

$$M_m = 1 - 2f_s T_d \quad (3)$$

where f_s is the switching frequency, $f_s = 1/T_s$. According to (3), the maximum linear modulation index M_m with varying T_d and f_s can be plotted in Fig. 4. As seen, M_m decreases with the increasing T_d and f_s . The influence of T_d on M_m at high switching frequencies, e.g. the M_m with T_d of $1\mu s$ can reach to 0.98 at 10kHz, but is reduced to 0.8 at 100kHz. The influence of the dead time and switching frequency on the linear modulation region indicates that, due to the indispensable dead time in the SRPWM, the linear modulation region of the SRPWM is smaller than that of the CDPWM, especially at high switching frequencies.

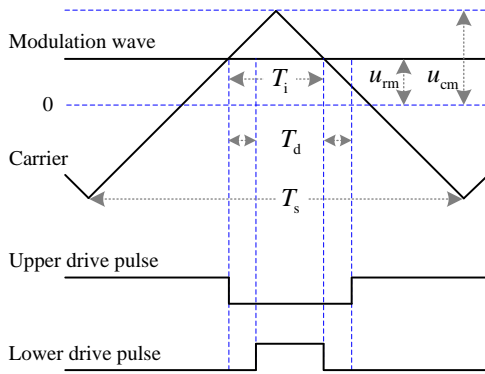


Fig. 3: With the SRPWM, the modulation at the top of the modulation wave in one switching cycle.

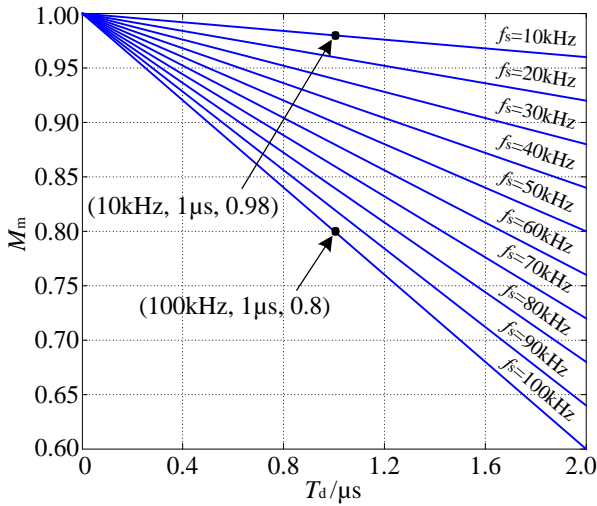


Fig. 4. M_m with varying T_d and f_s .

In addition, the dead time compensation for the SRPWM can only compensate the voltage losses caused by the dead time, but cannot extend the linear modulation region of the SRPWM. Conversely, the dead time compensation adjusts the amplitude of the modulation wave according to the current direction, which can increase the amplitude of the modulation wave with further decreased linear modulation region (inverter mode). Taking the switching frequencies of 10kHz and 100kHz for example, if the dead time of $1\mu s$ needs to be

compensated, the amplitude of the modulation wave should be adjusted by 0.02 and 0.2 ($u_{cm}=0.5$), respectively [8], [9]. It is indicated that, the dead time compensation at high switching frequencies will heavily affect the linear modulation region.

4 Control analysis of the CDPWM

The operation of the conventional SRPWM has nothing to do with the current direction, which makes it possible for the SRPWM to work at no-load state or in open-loop system. However, as with the dead time compensation in the SRPWM, the current direction is a prerequisite in the implementation of the CDPWM, making the CDPWM can only be implemented in closed-loop systems for practical applications [4], [7]. In this section, the current-direction-detection techniques for the CDPWM in closed-loop systems are discussed, and an open-loop control strategy without current-direction detection for the CDPWM is proposed for experimental purposes.

4.1 The current-direction-detection techniques for the CDPWM in closed-loop systems

The current-direction-detection techniques existing in the dead-time compensation can be adopted for distributing the drive pulses in the CDPWM, which can be grouped into three categories: (1) directly sensing the current direction by current sensors, (2) detecting the conduction of power devices by auxiliary circuits to obtain the current direction [7], [8], and (3) estimating the current direction from the load electrical angle [10]. The above current-direction-detection techniques are discussed as follows:

- 1) Regarding the method using current sensors, due to the current ripple and noise in actual currents, it is hard to accurately sense the current direction at the zero crossing, especially when the current is extremely small [7]. Using the conditioning circuits or the software-based low-pass filter can eliminate the current ripple and noise. However, a significant delay may be introduced to the sensed current, e.g. the delay caused by the conditioning circuit with the second order Butterworth low-pass filter can reach up to $100\mu s$ [11], which equals to the time of 10 switching cycles at the switching frequency of 100kHz.
- 2) Using the auxiliary circuit to detect the current direction, the delay in the sensed current direction can be effectively reduced, which is expected in high-switching frequency applications [8]. However, the current-direction detection with the auxiliary circuit is also susceptible to the ripple and noise at the current zero crossing when the current is extremely small. In addition, the auxiliary circuit has the galvanic isolation issue with increased complexity and cost of the system [7].
- 3) The method estimating the current direction from the load electrical angle can only be used in some particular cases. For example, in the permanent magnet synchronous motor (PMSM) drive system, the current direction can be estimated by the rotor position [10]. Besides, it is hard to guarantee the precision of the estimated current direction.

Apart from the above current-direction-detection techniques, the current reference in closed-loop systems can also be used to obtain the current direction [4]. The current reference has a better immunity to noise and no ripple at zero crossing. Applying the current direction obtained by the current reference to the CDPWM can make the converter work well at light-load state, where detecting the current direction is challenging. A drawback of using the current reference is that, the obtained current direction may be not as accurate as that directly sensed from the currents due to the control errors in closed-loop systems, especially in dynamic state. Nevertheless, considering the compromise between performance and complexity of the above methods, the current direction obtained from the current reference is preferred in the implementation of the CDPWM [4].

4.2 An open-loop control strategy for the CDPWM

In some experimental cases, e.g., testing the topology or efficiency of the converter, it is unnecessary to build the complicated closed-loop system, an open-loop experiment is sufficient for the test. Therefore, a simple open-loop control strategy without current-direction detection for the CDPWM is proposed in this paper for experimental purposes.

For a passive ac load, the phase angle between the current and voltage (power factor angle) is always constant. Therefore, if the power factor angle of the load has been known, the current direction can be calculated with the power factor angle and the modulation wave, which is similar to the method estimating the current direction from the load electrical angle [10]. Based on the above analysis, an open-loop control strategy for the CDPWM is proposed, and the flowchart is shown in Fig. 5. Firstly, the power factor angle of the passive load for experiments is estimated by measurement or calculation. Then, based on the estimated power factor angle and the modulation wave, the current direction can be calculated for the CDPWM implementation. Considering the errors in the obtained current direction, lastly, the obtained current direction need to be adjusted manually when operating, to minimize the current distortion at zero crossing.

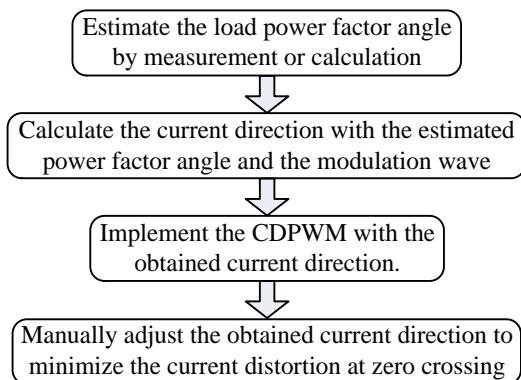


Fig. 5: Flowchart of the open-loop control strategy for the CDPWM.

It should be noted that, the requirement of the power factor angle of the complicated loads cannot be met in practical applications, where the implementation of the CDPWM should still be in closed-loop systems. In addition, the proposed open-loop control strategy for the CDPWM can also be adopted to the dead-time compensation in the SRPWM for experimental purposes, to avoid using the problematic current-direction detection.

5 Synchronous rectification in the split output converter

For the standard two-level voltage source converters, the efficiency with the SRPWM can be higher than that with the CDPWM due to the synchronous rectification can reduce the conduction losses in the current freewheeling stage [5]. In this section, the synchronous rectification in the split output converter will be tested by the double pulse test (DPT) on the designed circuit, to reveal how the split inductors affect the synchronous rectification.

Fig. 6 shows the designed three-phase split output converter based on the scheme in Fig. 1. The SiC MOSFET C2M0080120D (20A, 1200V, 80mΩ) and the SiC Schottky diode C4D20120A (20A, 1200V) both from Cree are adopted. The DPT is carried out on Phase C of the designed circuit respectively without and with the split inductors of 10μH. The freewheeling current in D₂ and Q₂ are measured and divided into three parts for clear descriptions, as shown in Fig. 7.

Fig. 7(a) shows the freewheeling currents without split inductors. In Part 1 and Part 3 of Fig. 7(a), the SiC MOSFETs Q₅ and Q₂ are both in off state, the freewheeling current only flows through the SiC Schottky diode D₂, and no current flows through the body diode of the SiC MOSFET Q₂ in steady state even with the rated current of 20A. It is indicated that, the forward characteristic of the SiC Schottky diode is much better than that of the body diode of the SiC MOSFET. In Part 2 of Fig. 7(a), when Q₂ turns on, the current freewheeled by D₂ is partly switched to the channel of Q₂, making the circuit in the synchronous rectification mode. The current is shared between the SiC Schottky diode D₂ and the channel of the SiC MOSFET Q₂.

Fig. 7(b) shows the results with split inductors of 10μH. In Part 1 and Part 3 of Fig. 7(b), there is a small current flowing through the body diode of Q₂ due to the current freewheeling caused by split inductors [3]. Meanwhile, in Part 2 of Fig. 7(b), the current flowing through the channel of Q₂ has become very small making the synchronous rectification mode almost disappear, which can be explained as follows. After Q₂ turns on, the circuit is in the synchronous rectification mode, where the current flowing through D₂ will fall while the current flowing through the channel of Q₂ will rise. However, the split inductors L_{s5} and L_{s2} shown in Fig. 1 can respectively counteract the falling and rising currents, leading to the almost disappeared synchronous rectification.

The DPT results indicate that, no matter the drive pulse of the lower SiC MOSFET Q_2 is high or low (SRPWM or CDPWM), the freewheeling current will almost only flow through the SiC Schottky diode D_2 in the split output converter. With the almost disappeared synchronous rectification, the split output converter with the SRPWM and the CDPWM can have the similar efficiency and device thermal swing.

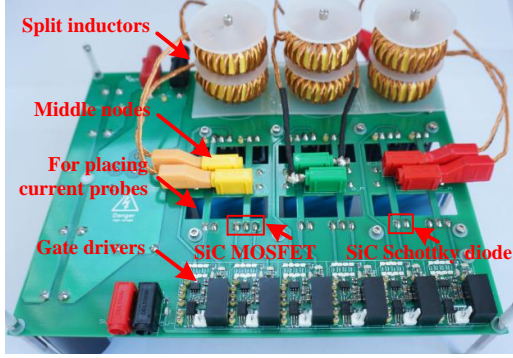


Fig. 6: Designed three-phase split out converter.

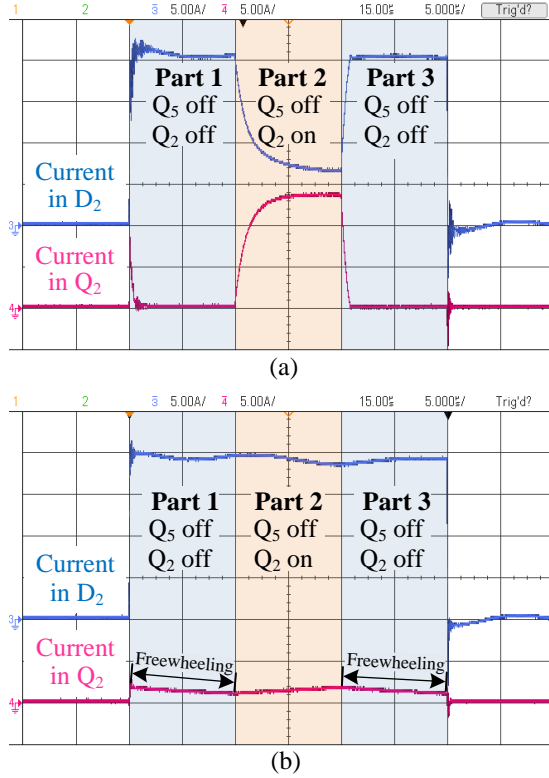


Fig. 7: Freewheeling currents in D_2 and Q_2 : (a) without split inductors and (b) with split inductors of $10\mu\text{H}$.

6 Experiments in continuous operating mode

The experiments in the continuous operating mode are further carried out based on the designed three-phase split output converters. The parameters of the test system are shown in Table 1. The SRPWM is implement by the conventional open-loop control, while the SRPWM with the dead time compensation and the CDPWM are implemented by the

proposed open-loop control strategy in Section 4.2. The three-phase currents with different PWM schemes are shown in Fig. 8. The corresponding total harmonic distortion (THD) of the currents is given in Table 2.

Symbol	Parameter	Value
V_{dc}	DC-link voltage	600V
R_L	Load resistance	44Ω
L_{load}	Load inductance	6.2mH
L_s	Split inductance	$10\mu\text{H}$
M	Modulation index	0.9
f_s	Switching frequency	100kHz
t_d	Dead time	$1\mu\text{s}$

Table 1: Parameters of the test system.

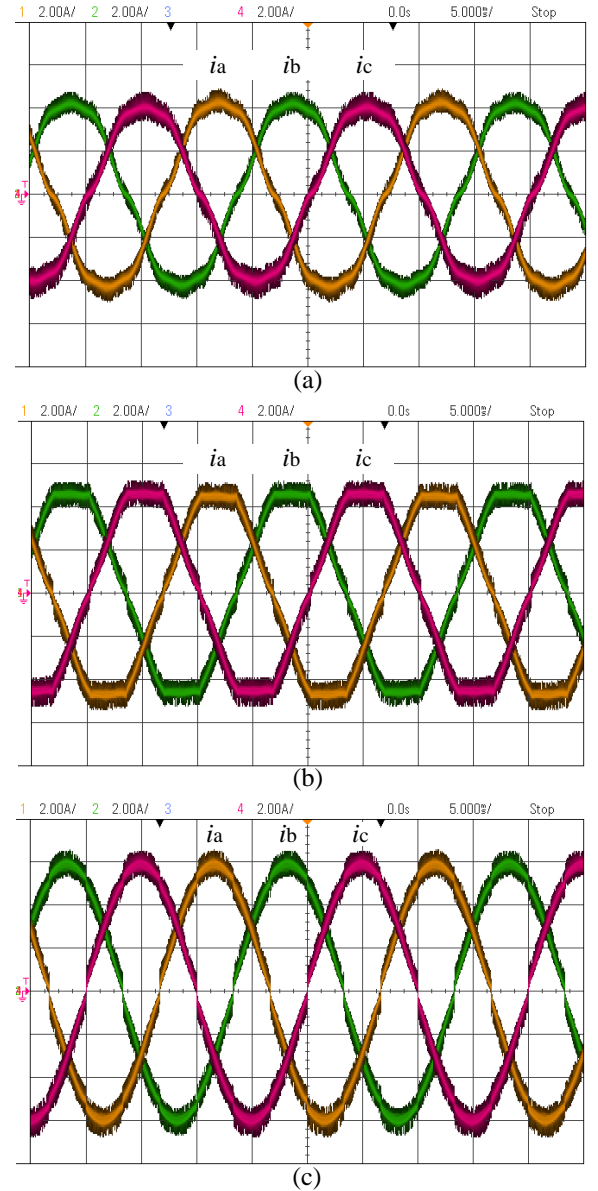


Fig. 8: Three-phase currents: (a) using the SRPWM, (b) using the SRPWM with the dead time compensation, and (c) using the CDPWM.

PWM scheme	THD of three-phase currents		
	i_a	i_b	i_c
SRPWM	6.86%	6.92%	7.16%
SRPWM with dead time compensation	5.88%	5.78%	6.01%
CDPWM	3.23%	3.14%	3.40%

Table 2: Current THD with different PWM schemes.

The dead time in the SRPWM can cause significant output voltage errors at high switching frequencies. And the SRPWM with $M=0.9$ and $f_s=100\text{kHz}$ makes the converter operate in the nonlinear modulation region, as analyzed in Section 3. Consequently, as see in Fig. 8(a) and Table 2, with the SRPWM, serious distortions appear in the three-phase currents with the highest THD.

Adopting the SRPWM with the dead time compensation, the THD of the output currents has been reduced compared to that without the dead time compensation, as seen in Table 2. However, the dead time compensation increases the amplitude of the modulation wave with intensified overmodulation, leading to the flattened top of the three-phase currents in Fig. 8(b).

The CDPWM without dead time will not generate the output voltage errors with high linear modulation region. As see in Fig. 8(c) and Table 2, compared with the above two PWM schemes, the three-phase currents with the CDPWM have the minimum distortion with the lowest THD, and only slight distortions happen at the current zero-crossing.

In addition, using the three PWM schemes with the same experimental parameters, the output powers are measured as 1307.21W, 1597.09W, and 2420.03W, respectively, which verifies the CDPWM without dead time has the highest dc-link utilization. And correspondingly, the efficiencies are measured as 95.91%, 95.97%, and 96.01%, respectively, which are very close. However, many factors, e.g. the operating power, can influence the converter efficiency, a more detailed investigation into the influence of the PWM schemes on efficiency should be further carried out.

7 Conclusion

The dead time in the SRPWM can cause output voltage errors and reduce the linear modulation region with lower dc-link voltage utilization. And the dead-time effect will be intensified as the switching frequency goes higher. Although the dead time compensation can eliminate the output voltage errors, due to the amplitude of the modulation wave can be increased by the dead time compensation, the linear modulation region of the SRPWM will be further decreased. Apart from the requirement of the current direction, the CDPWM without dead time is superior to the SRPWM with lower output current harmonics, larger linear modulation region, and higher dc-link utilization. In addition, due to the split inductors of the split output converter can make the synchronous rectification disappear, the converter with the CDPWM can have the similar efficiency as that with the

SRPWM. Overall, the CDPWM is a preferred choice for the SiC device based split output converters in high-switching-frequency applications.

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References

- [1] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.
- [2] VINCOTECH. (Oct. 2013). SiC MOSFET-based power modules utilizing split output topology for superior dynamic behavior. [Online]. Available: http://www.vincotech.com/fileadmin/user_upload/articles/bp_2013_10-SiC_MOSFET-based_Power_Modules.pdf
- [3] H. Li, S. Munk-Nielsen, S. Bęczkowski, and X. Wang, "SiC MOSFETs based split output half bridge inverter: current commutation mechanism and efficiency analysis," in *Proc. Energy Convers. Congr. and Expo.*, Pittsburgh, PA, Sep. 2014, pp. 1581–1588.
- [4] P. Sun, C. Liu, J.-S. Lai, C.-L. Chen, and N. Kees, "Three-phase dual-buck inverter with unified pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1159–1167, Mar. 2012.
- [5] W. Feng, F. C. Lee, P. Mattavelli, and D. Huang, "A universal adaptive driving scheme for synchronous rectification in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3775–3781, Nov. 2012.
- [6] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. New York: Wiley, 2003.
- [7] L. Chen and F. Peng, "Dead-time elimination for voltage source inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 574–580, Mar. 2008.
- [8] M. Ogawa, S. Ogasawara, and M. Takemoto, "A feedback-type dead-time compensation method for high-frequency PWM inverter — Delay and pulse width characteristics," in *Proc. IEEE 27th Appl. Power Electron. Conf. Expo.*, Orlando, FL, Feb. 2012, pp. 100–105.
- [9] A. Lewicki, "Dead-time effect compensation based on additional phase current measurements," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4078–4085, Jul. 2015.
- [10] H. Mese and A. Ersak, "Compensation of nonlinear effects in three-level neutral-point-clamped inverters based on field oriented control," in *Proc. IEEE 25th Power Electron. Motion Control Conf.*, Novi Sad, Sep. 2012, pp. DS2c.2-1–DS2c.2-8.
- [11] Q. Yan, X. Wu, X. Yuan, and Y. Geng, "An improved grid voltage feedforward strategy for high-power three-phase grid-connected inverters based on the simplified repetitive predictor," *IEEE Trans. Power Electron.*, 2015, DOI: 10.1109/TPEL.2015.2461632.